CLAIMS

1. A DC to DC converter circuit, comprising:

a comparator that is electrically coupled in said converter circuit so as to compare an output voltage of said converter circuit with a reference signal and generate a pulse width modulated signal;

a driver that is electrically coupled to said comparator so as to use said pulse width modulated signal as its input and drive a pair of switches, one high, one low, which alternatively control a level of said output voltage; and

a low pass filter that is electrically coupled to an output of said pair of switches so as to reduce noise of said output voltage;

wherein said comparator forces said output voltage at a pre-established value by increasing or decreasing the pulse width of said pulse width modulated signal when said output voltage is lower or higher than said pre-established value.

2. The DC to DC converter circuit of Claim 1, wherein said reference signal is generated by a reference signal generator that is coupled to a reference DC voltage source.

3. The DC to DC converter circuit of Claim 2, wherein said reference signal is a periodic signal of any shape with a DC offset determined by a DC voltage generated by said reference DC voltage source.

4. The DC to DC converter circuit of Claim 1, wherein each of said switches comprises a metal oxide semiconductor field effect transistor.

5. A two-phase DC to DC converter circuit, comprising:

a first phase circuit and a second phase circuit which are electrically coupled to each other;

wherein said first phase circuit comprises:

a first comparator which is electrically coupled in said two-phase DC to DC converter circuit so as to compare an output voltage of said first phase circuit with a first reference signal and generate a first pulse width modulated signal; and

a first driver which is electrically coupled to said first comparator so as to use said first pulse width modulated signal as its input and drive a first pair of switches, one high, one low, which alternatively control a level of said output voltage of said first phase circuit;

wherein said first comparator forces said output voltage of said first phase circuit at a first pre-established value by increasing or decreasing the pulse width of said first pulse width modulated signal when said output voltage of said first phase circuit is lower or higher than said first pre-established value; and

wherein said second phase circuit comprises:

a second comparator which is electrically coupled in said two-phase DC to DC converter circuit so as to compare an output voltage of said second phase circuit with a second reference signal and generate a second pulse width modulated signal; and

a second driver which is electrically coupled to said second comparator so as to use said second pulse width modulated signal as its input and drive a second pair of switches, one high, one low, which alternatively control the level of said output voltage; and

wherein said second comparator forces said output voltage of said second phase circuit at a second pre-established value by increasing or decreasing the pulse width of said second pulse width modulated signal when said output voltage of said second phase circuit is lower or higher than said second pre-established value; and

wherein said first reference signal and said second reference signal are shifted in phase by 180 degrees to each other.

6. The two-phase DC to DC converter circuit of Claim 5, further comprising:

a current balancing device which is electrically coupled in said two-phase DC to DC converter circuit so as to maintain the current delivered by said second phase circuit the same as the current delivered by said first phase circuit by modifying a reference voltage for said second phase circuit.

7. The two-phase DC to DC converter circuit of Claim 6, wherein said current balancing device comprises:

an offset voltage, which is used to adjust an output voltage of said second phase circuit; and

an error amplifier, which controls said offset voltage so as to change the duty cycle of said second phase circuit.

8. The two-phase DC to DC converter circuit of Claim 5, further comprising:

a current balancing device which is electrically coupled in said two-phase DC to DC converter circuit so as to maintain the current delivered by said second phase circuit the same as the current delivered by said first phase circuit by modifying a feedback voltage for said second phase circuit.

9. The two-phase DC to DC converter circuit of Claim 8, wherein said current balancing device comprises:

an offset voltage, which is used to adjust an output voltage of said second phase circuit; and

an error amplifier, which controls said offset voltage so as to change the duty cycle of said second phase circuit.

10. The two-phase DC to DC converter circuit of Claim 5, wherein said first reference signal and said second reference signal are generated by a reference signal generator which is coupled to a reference DC voltage source.

11. The two-phase DC to DC converter circuit of Claim 10, wherein each of said reference signals is a periodic signal of any shape with a DC offset determined by a DC voltage generated by said reference DC voltage source.

12. The two-phase DC to DC converter circuit of Claim 5, wherein each of said switches comprises a metal oxide semiconductor field effect transistor.

13. A converter circuit for a multiphase DC to DC converter circuit comprising N converter circuits which are electrically coupled together, said converter circuit comprising:

a comparator which is electrically coupled so as to compare an output voltage of said converter circuit with a reference signal and generate a pulse width modulated signal; and

a driver which is electrically coupled to said comparator so as to use said pulse width modulated signal as its input and drive a pair of switches, one high, one low, which alternatively control a level of said output voltage;

wherein said comparator forces said output voltage at a pre-established value by increasing or decreasing the pulse width of said pulse width modulated signal when said output voltage is lower or higher than said pre-established value; and

wherein each two reference signals are phase-shifted by 360/N degrees from each other.

14. A DC-to-DC converter, comprising:

a number of conversion circuits which are electrically coupled in said converter,

wherein each of said conversion circuits comprises:

a comparator which is electrically coupled so as to compare an output voltage of said converter with a reference signal and generate a pulse width modulated signal; and

a driver which is electrically coupled to said comparator so as to use said pulse width modulated signal as its input and drive a pair of switches, one high, one low, which alternatively control a level of said output voltage;

wherein said comparator forces said output voltage at a pre-established value by increasing or decreasing the pulse width of said pulse width modulated signal when said output voltage is lower or higher than said pre-established value; and

wherein each two reference signals are phase-shifted from each other with a degree of 360 divided by the number of conversion circuits coupled in said converter.

15. The DC-to-DC converter of Claim 14, further comprising:

a current balancing device which is electrically coupled in said multiphase DC to DC converter so as to maintain the currents delivered by all conversion circuits at a same level by modifying feedback voltages for the conversion circuits from second phase to N phase .

16. The DC-to-DC converter of Claim 14, further comprising:

a current balancing device which is electrically coupled in said multiphase DC to DC converter so as to maintain the currents delivered by all conversion circuits at a same level by modifying the reference voltages for the conversion circuits from second phase to N phase .

17. A method of producing a voltage output signal, comprising the steps of:

applying a reference signal to a converter circuit to produce a voltage output signal;

comparing said reference signal with said voltage output signal;

generating a pulse width modulated signal with a duty cycle determining an increase or decrease in said output voltage signal; and

forcing said voltage output signal at a pre-established value by increasing or decreasing the pulse width of said pulse width modulated signal when said output voltage signal is lower or higher than said pre-established value respectively;

wherein said converter circuit comprises:

a comparator which is electrically coupled in said converter circuit so as to compare the output voltage of said converter circuit with said reference signal and generate said pulse width modulated signal; and

a driver which is electrically coupled to said comparator so as to use said pulse width modulated signal as its input and drive a pair of switches, one high, one low, which alternatively control the level of said output voltage.

18. The method of Claim 17, wherein said reference signal is generated by a reference signal generator which is coupled to a reference DC voltage source.

19. The method of Claim 18, wherein said reference signal is a periodic signal of any shape with a DC offset determined by a DC voltage generated by said reference DC voltage source.

20. The method of Claim 17, wherein each of said switches comprises a metal oxide semiconductor field effect transistor.

21. The method of Claim 17, wherein said converter circuit comprises more than two sub-systems coupled together; and

discharging said capacitor with a constant current which is proportional to said input voltage while said switch is open.

wherein each of said sub-systems comprises:

a comparator which is electrically coupled so as to compare the output voltage of said converter circuit with a reference signal and generate a pulse width modulated signal; and

a driver which is electrically coupled to said comparator so as to use said pulse width modulated signal as its input and drive a pair of switches, one high, one low, which alternatively control the level of said output voltage; and

wherein each two reference signals are phase-shifted by 360/N degrees from each other.

22. A method for compensating an output voltage of a DC-to-DC converter with an input voltage, comprising the steps of:

generating a saw tooth voltage signal with an amplitude which is proportional to said input voltage; and

maintaining the maximal voltage value of said saw tooth signal at a fixed DC voltage level.

23. The method of Claim 21, further comprising the step of:

applying a set of clock pulses to a switch;

charging a capacitor to the maximal voltage value of said saw tooth signal while said switch is closed; and